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High Speed ALU for High Speed Processor Using C-Element

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***Abstract*— Asynchronous design provides a platform to overcome the drawback of synchronous design such as global worst-case latency, clock distribution and skew problem. In the VLSI design area, power and speed are the major factors to be considerable. So, in order to improve the speed we have to concentrate on delay. In this manuscript an asynchronous ALU is designed using a Muller C-element concept to reduce delay in the circuit.**

***Keywords* – ALU, Delay, Muller C-Element, Pipeline.**

I. INTRODUCTION

The majority of logic systems are based on the synchronous principle because of design simplicity using discrete time, which avoids the hazards. On the other side there are problems with global clock distribution, which leads to skew problem. Furthermore, the necessity of time analysis to ensure stability is the next problem. This is not an issue in asynchronous systems, which are clocked locally. Individual parts communicate locally only in necessary case. This communication is called handshaking where also exists the necessity of hazard avoidance. The asynchronous systems benefits are following [3]:

- Low-power consumption due fine-grain clock gating and zero stand-by consumption.
- High operating speed by actual local latencies rather than global worst-case latency.
- Less electro-magnetic emission due local clocks tend to tick random points in time.
- Better composability and modularity because of the simple handshake interface and the local timing.
- No clock distribution and skew problems.

This communication is called handshaking where also exists the necessity of hazard avoidance. However, even these classes of asynchronous logic become vulnerable because certain timing assumptions commonly accepted under normal operating conditions are no longer valid.
In particular, the delay of inverters, often used as the so-called input 'bubbles', can no longer be neglected and they have to be either removed or properly acknowledged to ensure speed-independence. High operating speeds by actual local latencies rather than global worst-case latency-paths, In contrast with synchronous circuits asynchronous are controlled by locally derived clocks. Handshaking ensures that clock pulses are generated whenever and wherever they are needed. Fig. 1 shows generalized asynchronous circuit with request, acknowledgement handshaking and with level-sensitive latches in data path [3].

The rest of the paper has organized as follows. Section II Explains briefly about the design of 4-bit ALU used. Section III describes the Muller C element. Section III. Section IV shows the simulation results and shows delay comparison of the proposed design with existing designs.

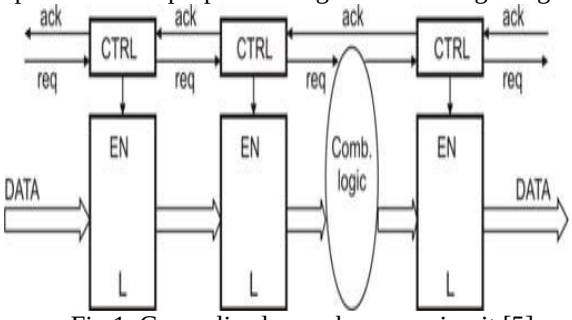

Fig.1. Generalized asynchronous circuit [5]

II. DESIGN OF ALU

Several researchers propose asynchronous approaches to cope with performance and timing issue. Tang et. al. designed a 16-bit asynchronous ALU with an asynchronous pipeline architecture [1]. In this approach, simple handshake cells embedded in pipeline stages make the ALU run fast. However, large power has consumed by this design while waiting for the incoming data. In contrast, by using Galois Field arithmetic logic and reduced switching activity in the latches, paper [2] achieved low power in their asynchronous ALU design. Several researchers propose asynchronous approaches to cope with performance and timing issue. Tang et. al. designed a 16- bit asynchronous ALU with an asynchronous pipeline architecture [1]. In this approach, simple handshake cells embedded in pipeline stages make the ALU run fast. However, large power has consumed by this design while waiting for the incoming data.

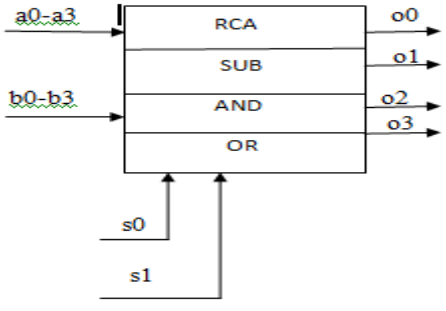

Fig.2. 4 Bit ALU

Fig.2 shows the block representation of 4 bit alu having the 4 operations with two selection lines and two 4 bit input (a,b), can done such operation **adder, subtractor, and, or**. Using a selected lines (s0,s1) .we can choose the operation randomly show the **Table.1.** the outputs are (o0-o3).

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Table 1: ALU operation

S0	S1	OPERATION
0	0	ADDER
0	1	SUBTRACTOR
1	0	AND
1	1	OR

In contrast, by using Galois Field arithmetic logic and reduced switching activity in the latches.

III. MULLER C-ELEMENT

The Muller C-element or Muller C-gate, is a commonly used logic component originally designed by David E. Muller [6]. In synchronous systems the signal is valid only if clock transitions otherwise it may be various. In asynchronous systems the signal has to be valid all the time, therefore the hazard avoidance is critical. In Boolean gates the input signals cannot be determined with certainty on the basis of output signal. E.g. OR gate output is '0' when both inputs are '0'. But output in '1' does not say whether input is in '1' or '0'. This problem is solved with a new part: a Muller C-element. It is fundamental element in asynchronous circuits.

Table.2. shows truth table. If output is '1' inputs are both '1'. When output is '0' then both inputs are '0'. Other combinations on inputs cause no change on the output, because of feedback from output showed in schematic.

Table 2 : Truth table of C-element [5]

A	B	Y
0	0	0
0	1	No change
1	0	No change
1	1	1

Signals arrive on inputs in different times. This C-element indicates, when both signals arrive on the inputs. The symbol and Boolean gates schematic of C-element are presented in Fig.3.Following equation describes this element.

$$y = a.b + y.(a + b).$$

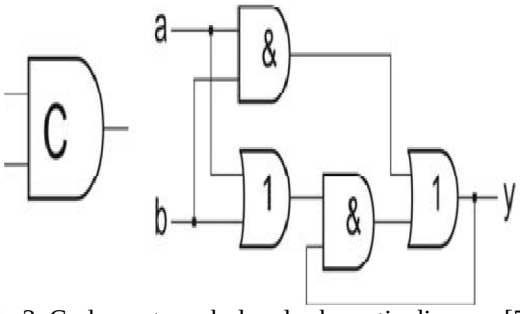

Fig.3. C-element symbol and schematic diagram [5]

The Muller C-element is a fundamental circuit element widely used for control synchronization in asynchronous designs. In general, a C-element is a state holding circuit which is transparent when all its inputs are equal, and holds the previous output otherwise. C-elements are so important in asynchronous design, we study their sensitivity to particle strike, and discuss the optimization techniques to increase their soft error tolerance. In this paper, four static single rail C-element implementations are taken for analysis one of the C-element implementation with conventional pull-up and pull-down circuit followed shows the C-element implementation with an inverter latch and with a modified inverter latch. Because of having an advantages in Muller- c element. By applying this Muller c-element as a input component for 4 bit alu circuit i.e. Instead of applying the input in a direct flow, we pass it through the Muller c-element. By this we reduced the delay of the overall circuit when compare it with the previous one. The simulation results are shown below by using Xilinx ISE 12.1 and model sim.

A. MULLER PIPELINE

Pipeline from C-elements creates the Muller pipeline, see Fig. 4. The Muller pipeline is a backbone of all asynchronous systems in a number of variations. The principle is that element C[i] receive '1' from its predecessor C [i-1] only if its successor C[i+1] contains '0'. Likewise element C[i] receive '0' from its predecessor C [i- 1] only if its successor C[i+1] contains '1'. This pipeline transfers handshaking. If handshaking is inserted on the left side of the pipeline, they will propagate to the right side. If no ack comes from the right environment, pipeline will fill up and after some time it will be stopped [3]. The interesting property of this important part is symmetry. It works as well as from left to right as from right to left, but with reversed signals. Second characteristic is delay-insensitivity. The 4-phase or the 2-phase protocol can be used. Possible implementations are 4-phase bundled-data, 2-phase bundled-data and 4-phase dual-rail.

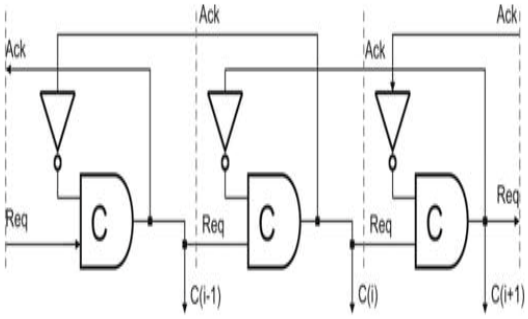

Fig.4. Muller pipeline [5]

IV. SIMULATION RESULTS

The Simulation result for 4-bit ALU is show below. It consists of two arithmetic operation such as adder, subtraction and two logical operation such as AND, OR operation are shown below. By using the Muller C element the progation delay is reduced. Table 3 shows the delay comparison of 4 bit ALU with and without using Muller C element.

The four bit Ripple carry adder and four bit subtraction circuit is used in the arithmetic unit and the four bit ADD and OR operation is performed in the logical unit. By using the modelsim simulator the operation of the ALU circuit is simulated and shown below.

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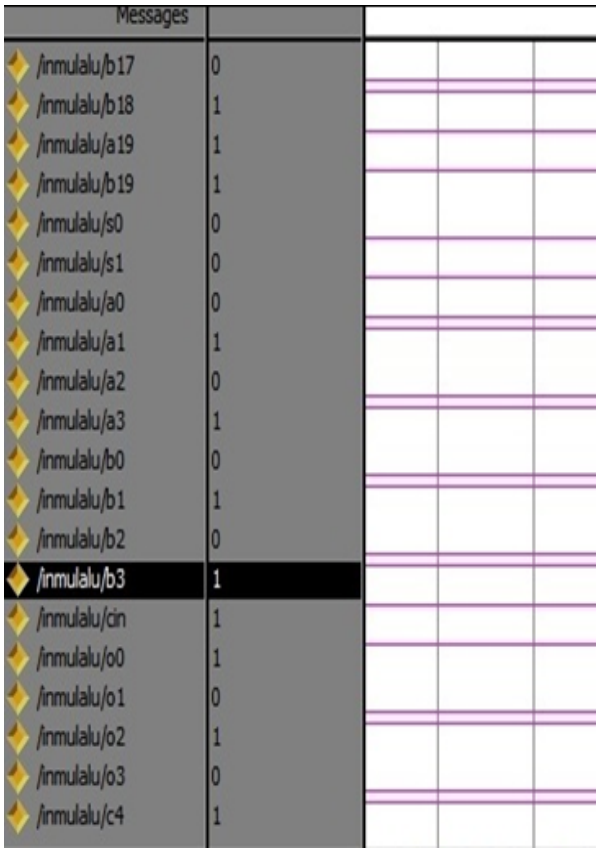
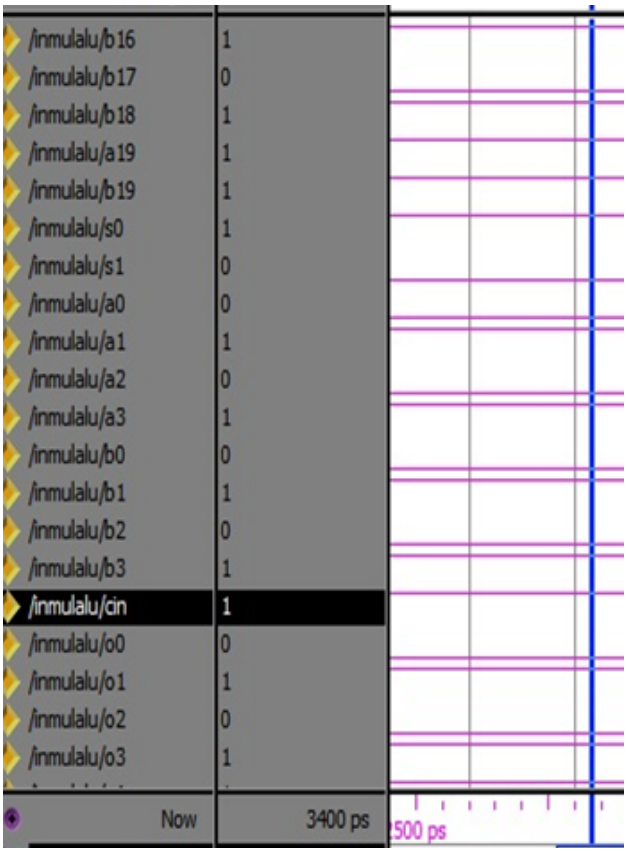
A. ADDER OPERATION



B. SUBTRACTOR OPERATION

C. AND OPERATION



D. OR OPERATION

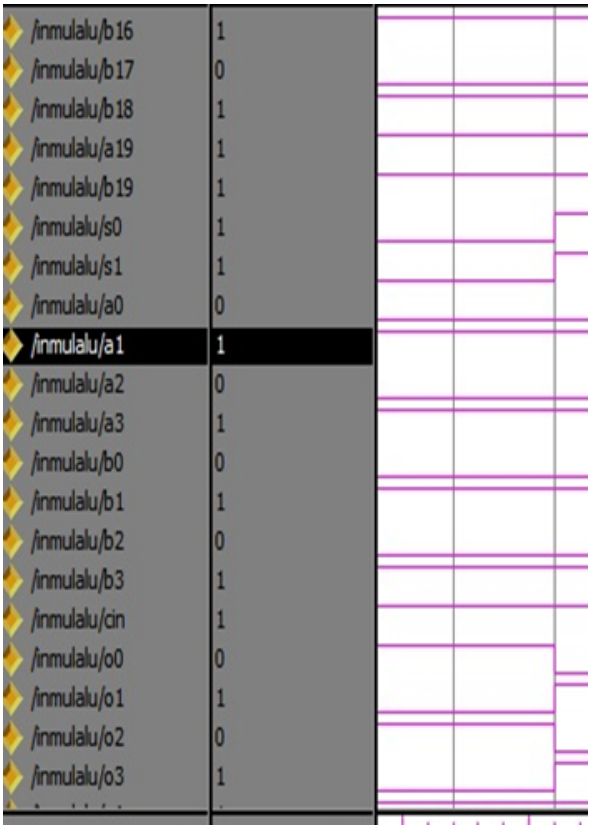


Table 3: Delay comparison table

	Conventional System	Proposed System
BEFORE CLK	8.269ns	7.521ns
AFTER CLK	4.368ns	4.114ns
PATH ANALYSIS	10.504ns	10.058ns

V. CONCLUSION

The fundamentals of asynchronous logical systems and Muller c-element were presented at beginning of this article. And the simulation model of normal 4 bit ALU and Muller c- element based 4 bit ALU were simulated and described. The aim of this work is to design the circuits with least delay. There by we reduced the delay by using the Muller c-element in the 4 bit ALU circuit.

ACKNOWLEDGEMENT

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